# GEORGIA INSTITUTE OF TECHNOLOGY School of Electrical and Computer Engineering ECE 2020 Lab #2: Finite State Machines

This lab is due one week from the day it is assigned in class. You may work in groups of two and share a checkoff sheet, however you are expected to print your own checkoff sheet and bring it to class.

# GOAL

The goal of this experiment is to reinforce state machine concepts by having students design and implement a state machine using simple chips and a protoboard. This experiment also introduces students to basic physical components.

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# **EQUIPMENT NEEDED**

- NAND gate (SN74LS00N)
- NOT gate (SN74LS04NE4)
- D-flip flop (SN74HC74N)
- 3-to-8 line decoder (TC74HC138APF)
- Jumper wires
- Breadboard
- myDAQ

# BACKGROUND

**States:** A = 00, B = 01, C = 10, D = 11 where the states are defined by the values stored in the registers; for example, State B corresponds to  $S_1S_0 = 01$  where  $S_1$  is the value of Register 1 and  $S_0$  is the value of Register 0. The next state for values of the registers is defined by NS<sub>1</sub> for Register i. For example, if the current state is B and the next state is C, then  $S_1S_0 = 01$  and  $NS_1 = 1$  and  $NS_0 = 0$ .

*External input:* The external input in this circuit is denoted as "X".

**3-to-8 Decoder:** Signals  $A_0 - A_2$  represent the inputs and  $Y_0 - Y_7$  represent the outputs. The convention is that  $A_2$  represents the most significant bit of a binary number and  $A_0$  represents the least significant bit; for example, an input of 011 is designated as  $A_2A_1A_0 = 011$ . The 74138 decoder has **inverted** outputs so take that into account in your design.



Figure 1. Diagram of 3-to-8 Decoder

*Pin Connection Diagram:* It is critically important you label your diagram with pin and package numbers. You will have 3-5 ICs on the board, each needing power and ground, with multiple wires connecting each. Without labelling your pins ahead of time, it will be hard to construct and even harder to troubleshoot.

#### **PRE-LAB PROBLEMS**

1) Fill out the truth table on the next page for the given state machine:



STATE	Sı	S <sub>0</sub>	Х	NEW STATE	NS1	NS₀
Α	0	0	0			
Α	0	0	1			
	0	1	0			
	0	1	1			
	1	0	0			
	1	0	1			
	1	1	0			
	1	1	1			

- 2) Draw the circuit for your state machine below (see Figure 3 in the Lab Procedures section if you need help getting started). Some tips for selecting the gates:
  - a) Decoders using inverted outputs and NANDs are functionally the same as decoders using non-inverted outputs and ORs.
  - b) NANDs can be used as inverters (by shorting the two inputs)

### LAB PROCEDURES

- 1. Initial steps
  - a. It is helpful to make a habit of connecting your Vcc and ground to the buses of your breadboard. Connect +5V to the + buses and DGND to the – buses. Since some of these chips have connections that have to be made on both sides, it is helpful to have both Vcc and ground on both the top and the bottom of the board.
- 2. Setting up the decoder
  - a. Insert the decoder into your breadboard and connect Vcc and GND. Since this circuit has many connections, these "standard" connections should be as out of the way as possible. Use the smallest wires that will connect the pins. These wires should be nearly flush with the breadboard.
  - b. This decoder has 3 enable pins, two enable low, one enable high. The E pins need to be connected to ground (enable low) and the E pin needs to be connected to Vcc. Since the decoder will always be enabled for this lab, use as short wires as possible to keep them out of your way.
  - c. The decoder is now powered and enabled. You can test it by giving it a three-bit input to A0, A1, and A2 and observing the outputs Y0-Y7. Remember, the 74138 gives **inverted outputs** which means that all outputs but the one selected will output a high voltage. This makes it easy to connect to NAND and NOR gates.
  - d. For these state machines, we will be giving a single bit as input from the myDAQ. Connect one of the digital output pins of the myDAQ (DIO0-3) to A0. The other two inputs will come from the current state.
- 3. Connecting the D flip flop
  - a. Insert the D flip flop (7474) IC into the breadboard. In order to simply the wiring, it may be wise to leave room between the two for any logic chips you use in your design.
  - b. Connect Vcc and ground.
  - c. We will not be using the preset pins PRE so we will connect these to Vcc. If we wanted the option to preset the D-flip flops to 1, we could bring this pin of the D-flip flop low.
  - d. We will be using digital I/O pins of the myDAQ to act as the clock and clear/reset. Connect both the CLK and CER to unused DIO pins. Remember, since the this is inverted clear, we need to keep that pin at 1 unless we want to reset both flip flops to zero, in which case we will change the input to 0.
  - e. Now the flip flop is powered and functional.
- 4. Building the Example State Machine (3 state)
  - a. The state transition diagram for this state machine is shown in Figure 2 on the next page.



Figure 2. State Transition Diagram

b. The truth table is shown below

State	S <sub>1</sub>	S <sub>0</sub>	Х	New State	$NS_1$	$NS_0$
Α	0	0	0	В	0	1
Α	0	0	1	А	0	0
В	0	1	0	С	1	0
В	0	1	1	А	0	0
C	1	0	0	С	1	0
C	1	0	1	А	0	0
	1	1	0			
	1	1	1			

c. Label the pins you are going to use on the schematic in Figure 3 below.



Figure 3: Circuit Diagram for Example State Machine (note: Vcc, ground, etc. are not shown)

- d. Insert NAND IC (7400)
- e. Connect Vcc and ground.
- f. Using the pin diagram, make the needed connections.
- g. Don't forget that the decoder is using inverted outputs!
- h. Test the state machine using the state transition diagram (Figure 2).
- i. Fill out Table 1 found in the Checkoff section as you walk through it with the TA.
- 5. Building the Pre-Lab State Machine (4 state)
  - a. Make sure that you label your pins before you start wiring everything. This will ensure that you don't mix up your wiring and the TAs can follow along with what you have done.
  - b. Be sure to connect Vcc and ground.
  - c. Don't forget that the decoder is using inverted outputs!
  - d. Test the state machine using the state transition diagram you filled out in the Pre-Lab section.
  - e. Fill out Table 2 found in the Checkoff section as you walk through it with the TA.



NAND Gate IC (74HC00) or (SN74LS00N):

# NOR Gate IC (74HC02) or (SN74LS02N):



NOT Gate IC (74HC04) or (SN74LS04N):



#### Register (D-FlipFlop) IC (74HC74):





### **APPENDIX B: Check-off Sheet**

(These tables should not be filled out until your TA is present and you are showing them your circuit)

Table 1:

State	Input	State												
Α	0		1		1		0		0		0		1	

TA Initials: \_\_\_\_\_

Table 2:

State	Input	State												
Α	0		1		1		1		0		1		1	

TA Initials: \_\_\_\_\_